Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. The original filing indicated that the square-bracketed cross-referencing numbers are not to be regarded as part of the claims, thus such square-bracketed cross-referencing material have been removed as shown in the below claims listing:

CLAIMS LISTING (all of pending claims 1-16)

Claim 1 (*Previously Presented*): A Programmably-Sliceable Switch-fabric Unit (PSSU) having a capability of functioning as an NxN' crossbar, and also having a capability of being programmably sliced to instead function as a plurality of SxS' virtual switch slices, where S<N and S'<N', wherein N does not have to equal N', and S does not have to equal S',

said PSSU comprising:

(a) absolute Ingress ports (aI's) and absolute Egress ports (aE's) that are alternatively identifiable as Relative ingress ports (Ri's) and Relative egress ports (Re's) of respective ones of said virtual switch slices; where the aI's can receive routing requests and payloads that are to be routed, and where the aE's can output routed payloads to corresponding destinations; and

(b) a request translator, operatively coupled to the aI's for receiving routing requests from the aI's, said request translator having:

(b.1) first means for determining, based on the absolute Ingress port identification (aI_x) of an ingress port on which a given request arrived, what virtual switch slice a corresponding payload signal belongs to;

(b.2) second means for determining from a Relative egress port identification (Re) or ports identifications (Re's) specified directly or indirectly in the given request, and from the identification of the virtual switch slice

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provided by said first means, which absolute Egress port (aE) or absolute Egress ports (aE's) the corresponding payload signal is to egress from in accordance with the given request; and

(b.3) third means for altering the given request before the request is submitted to a scheduler so that the altered request asks for egress of the corresponding payload signal from said determined aE or aE's.

Claim 2 (*Previously Presented*)**:** A machine-implemented method that is carried out in a Programmably-Sliceable Switch-fabric Unit (PSSU) having a capability of functioning as an NxN' crossbar, where said method gives the PSSU a capability of being programmably sliced to instead function as a plurality of SxS' virtual switch slices, where S<N and S'<N', wherein N does not have to equal N', and S does not have to equal S', where the PSSU includes absolute Ingress ports (aI's) and absolute Egress ports (aE's) that are alternatively identifiable as Relative ingress ports (Ri's) and Relative egress ports (Re's) of respective ones of said virtual switch slices; where the aI's can receive routing requests and payloads that are to be routed, and where the aE's can output routed payloads to corresponding destinations; and where said method comprises:

(a) receiving routing requests from the aI's

(b) first determining, based on the absolute Ingress port identification (aI_x) of an ingress port on which a given request arrived, what virtual switch slice a corresponding payload signal belongs to;

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(c) second determining from a Relative egress port identification (Re) or from Relative egress ports identifications (Re's) specified directly or indirectly in the given request, and from the identification of the virtual switch slice provided by said first determining step, which absolute Egress port (aE), or ports (aE's) the corresponding payload signal is to egress from in accordance with the given request; and

(d) altering the given request before the request is submitted to a scheduler so that the altered request asks for egress of the corresponding payload signal from said determined aE or aE's.

Claim 3 (*Original*): A machine-implemented method for using a Programmably-Sliceable Switch-fabric Unit (PSSU) that has a capability of functioning as an NxN' crossbar, and also has a capability of being programmably sliced to instead function as a plurality of SxS' virtual switch slices, where S<N and S'<N', and where the PSSU includes absolute Ingress ports (aI's) and absolute Egress ports (aE's) that are alternatively identifiable as Relative ingress ports (Ri's) and Relative egress ports (Re's) of respective ones of said virtual switch slices; where the aI's can receive routing requests and payloads that are to be routed, and where the aE's can output routed payloads to corresponding destinations;

said machine-implemented, usage method being carried out when the PSSU is functioning as said plurality of SxS' virtual switch slices, and the method comprising:

(a) determining if an ingress-related error rate exceeding a predefined and corresponding threshold is observed for requests and/or payloads arriving through a given ingress port;

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(b) if the exceeding error rate is observed, determining which virtual switch slice is associated with the given ingress port whose ingress-related error rate is exceeding the predefined and corresponding threshold, and disabling that virtual switch slice.

Claim 4 (*Previously Presented*): A request translation method for use in a system where absolute Ingress ports (aI's) and absolute Egress ports (aE's) are alternatively identifiable as Relative ingress ports (Ri's) and Relative egress ports (Re's) of respective, switch slices, and where the translation method comprises:

(a) determining, based on the absolute Ingress port identification (aI_x) of the port on which a given request arrived, what slice a corresponding payload signal belongs to;

(b) determining from a Relative egress port identification (Re) or Relative egress ports identifications (Re's) specified in the given request, which absolute Egress port (aE) or absolute Egress ports (aE's) the corresponding payload signal will egress from; and

(c) altering the given request so as to cause the corresponding payload signal to egress from said determined aE or aE's.

Claim 5: (*Canceled*).

Claims 6-8: (*Canceled*).

Claim 9 (*Original*): A monolithically integrated switch-fabric circuit comprising:

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(a) a plurality of ingress ports, where each ingress port is adapted to receive ingressing request signals that request switching of a corresponding payload signal, and where each ingress port is further adapted to receive ingressing payloads which are to be switched in accordance with corresponding ones of the request signals;

(b) a plurality of egress ports, where each egress port is adapted to output switched ones of said ingressing payloads, where identification of which egress port is to output which of the ingressing payloads is provided by egress identification indicia included in said ingressing request signals and the egress identification indicia provides said identification by way of at least one of:

(b.1) a direct and absolute identification (aE_x) of a respective one or more of the egress ports that are to output corresponding ones of the switched payloads;

(b.2) a direct and relative identification (Re_x) of a respective one or more of the egress ports that are to output corresponding ones of the switched payloads, where the direct and relative identification (Re_x) is based on a switch slice that is assumed to be coupled to the ingress port through which the corresponding request signal ingressed;

(b.3) an indirect, but nonetheless absolute identification (aE_x) of a respective subset of the egress ports that are to multicast out a corresponding one of the switched payloads; and

(b.4) an indirect and relative identification of a respective subset of the egress ports that are to multicast out a corresponding one of the switched payloads, where the indirect and relative identification is

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based on a switch slice that is assumed to be coupled to the ingress port through which the corresponding request signal ingressed;

(c) pre-switch, signal processing resources coupled to the plurality of ingress ports for processing at least said ingressing request and payload signals;

(d) post-switch, signal processing resources coupled to the plurality of egress ports for processing at least said switched and egressing payload signals;

(e) a switch matrix interposed between said pre-switch and post-switch, signal processing resources for switching corresponding ones of ingressing payloads that have been processed by the pre-switch, signal processing resources for egress through the post-switch, signal processing resources and through request-identified ones of said egress ports;

(f) a request translator operatively coupled to the egress ports for receiving the egress identification indicia which represent at least one of said direct and relative identifications (Re_X) and said indirect and relative identifications, and for producing translated, egress identification signals that provide absolute identifications of the egress ports through which egress of corresponding payloads is being requested by the corresponding ingressing request signals.

Claim 10 (*Original*): The monolithically integrated switch-fabric circuit of Claim 9 wherein said pre-switch, signal processing resources provide at least four of the following pre-switch, signal processing functions:

(c.1) level-shifting;

(c.2) bit-detection;

(c.3) clock recovery for asynchronously communicated signals;

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(c.4) conversion from a relatively serial format to a more parallel data format;

(c.5) signal framing;

(c.6) error checking and/or correction;

(c.7) ingress-side error logging for identifying ingress links that are currently error-prone;

(c.8) signal decoding or decompression;

(c.9) storage of ingress signal data; and

(c.10) alignment of received ingress signals with internal clocks of the switch-fabric circuit.

Claim 11 (*Original*): The monolithically integrated switch-fabric circuit of Claim 9 wherein said post-switch, signal processing resources provide at least four of the following post-switch, signal processing functions:

(d.1) encoding and/or compression of egressing payload signals;

(d.2) attachment of error correction and other control signals or framing signals to the egressing payload signals;

(d.3) egress-side error logging for identifying egress links that are currently error-prone;

(d.4) phase-alignment of egressing signals to external output clock signals if synchronous communication is being used;

(d.5) serialization of egressing signals;

(d.6) level-shifting of egressing signals; and

(d.7) transmission of grant and/or protocol signals as may be appropriate in accordance with protocols used by systems with which the switch-fabric circuit communicates.

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Claim 12 (*Previously Presented*): The monolithically integrated switch-fabric circuit of Claim 9 wherein said request translator comprises:

(f.1) a resource parser for determining whether received request signals are asking for multicast output of corresponding payloads or unicast output of corresponding payloads and for providing a first mode signal indicating whether a correspondingly-parsed request signal is of the unicast type or multicast type;

(f.2) a multicast lookup table for converting multicast egress codes into corresponding, specific multicast identifications of specific, relative egress ports from which a corresponding payload is to be output;

(f.3) a multicast mode translation block, coupled to the multicast lookup table, for converting the specific multicast identifications of said specific, relative egress ports into absolute multicast identifications; and

(f.4) a unicast mode translation block, coupled to the resource parser, for converting unicast type, relative identifications (Re_X) into absolute egress identifications.

Claim 13 (*Original*): The monolithically integrated switch-fabric circuit of Claim 12 wherein said request translator further comprises:

(f.5) a slicing pattern register for indicating what pattern of virtual switch slices is being implemented in the switch matrix; and

(f.6) a source port indicator for indicating what absolute ingress port (aI_X) a corresponding request signal came from;

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wherein each of the multicast mode translation block and the unicast mode translation block is coupled to, and responsive to outputs of the slicing pattern register and of the source port indicator.

Claim 14 (*Original*): The monolithically integrated switch-fabric circuit of Claim 13 wherein said request translator further comprises:

(f.7) an on-the-fly controlled multiplexer, coupled to outputs of the multicast mode translation block and of the unicast mode translation block, and driven by said first mode signal for selectively outputting on-the-fly, at least one of the outputs of the multicast mode translation block and of the unicast mode translation block.

Claim 15 (*Original*): The monolithically integrated switch-fabric circuit of Claim 13 wherein said multicast mode translation block performs a variable shift operation dependant on said outputs of the slicing pattern register and of the source port indicator.

Claim 16 (*Original*): The monolithically integrated switch-fabric circuit of Claim 13 wherein said multicast mode translation block selects amongst a plurality of spread-and-shift operations dependant on said output of the slicing pattern register.

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